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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,673	11/13/2003	David Zimmerman	5038-299	9857

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,673	ZIMMERMAN, DAVID	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-34* is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☒ Claim(s) *3 and 10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 822004, 040605
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-34 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 04/06/2005.

Information Disclosure Statement (IDS) filed on 02/20/2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Regarding claim 2, line 1, should be changed "the master memory buffer" to – a master memory buffer--.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2,4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Bechtolsheim et al. (U.S. Patent No. 5,973,951).

Regarding claim 1, Bechtolsheim et al. disclose a buffered memory module test (Figure 1a) fixture comprising:

a circuit board (5) having a first electrical connector (30) to receive a first buffered memory module under test,

a master memory buffer connection point (21, Column 3, lines 35-50), and

a first set of electrical traces (Column 3, lines 50-65) corresponding to a first point-to-point memory channel connecting the electrical connector with the master memory buffer connection point; and

a control bus (Column 3, lines 35-40) routed to the master memory buffer connection point, to propagate control signals to a master memory buffer to cause the master memory buffer to exercise the memory channel (Column 3, lines 55-67).

Regarding claims 2, 4-9, Bechtolsheim et al. disclose a master memory buffer (Figure 1a, 15), and wherein the master memory buffer is mounted to the circuit board (Figure 1a, 15), and wherein the master memory buffer connection point is a memory module electrical connector, and wherein the master memory buffer is mounted on a master memory module card inserted into the memory module electrical connector(Column 4, lines 32-60), and wherein the master memory module card further comprises a plurality of memory devices connected to the master memory buffer by a memory device channel (Figure 1a) and wherein the control bus is a system

management bus (Figure 1a, 25,20,21, Column 3, lines 30-55), and wherein the circuit board is configured for edge insertion in a computer peripheral bus slot, with the system management bus routed to the insertion edge of the card for connection to a computer system management bus (Figure 2a, 50), and further comprising at least one voltage regulator to supply operating power to a memory module and a master memory buffer during test, and a clock generator to supply a reference clock signal to the memory module and the master memory buffer during test (Column 1, lines 35-37, Column 2, lines 44-48. Figure 3, Column).

Allowable Subject Matter

8. Claims 3, 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 10-14 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Bechtolsheim et al. (U.S. Patent No. 5,973,951), and others, does not teach the claimed invention having a master memory buffer has a host-side memory port. And wherein the host-side memory port is disconnected, and a module circuit board having a set of memory device channel traces with a take-off point for monitoring signals on at least selected memory device channel traces.

9. Claims 15-34 are allowed.

Claims 15-34 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Bechtolsheim et al. (U.S. Patent No. 5,973,951), and others, does not teach the claimed invention having a memory module buffer comprises a control circuitry to cause the memory module buffer to send and receive memory channeldata over the downstream memory channel port in response to the test commands received at the control bust port as claims 15-20 disclosed, and a method of testing a memory channel independent of a host memory channel as claims 21-30 disclosed, and a computing device having test circuitry on the first buffered memory module to receive commands over the low-speed bus and respond by issuing memory commands over the second point-to-point memory channel to the second buffered memory module as claims 31-34 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER